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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,512	OSONE ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) ~~(PTO-1449)~~ Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 9 does not include reference sign "7." A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Figure 10, reference characters 14-16 and 10 have each been used to designate different parts with the same number. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim 11 feature, ""wherein areas, which emitter fingers except emitter fingers at both ends of the emitter fingers electrically connected by the same emitter wirings occupy in a plane orthogonal to the thickness-wise direction of the semiconductor substrate and the wiring board, are included in areas, which the through holes in the wiring

board occupy," must be shown or the feature canceled from the claim. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The unenabled subject matter is the claim 11 limitation, "wherein areas, which emitter fingers except emitter fingers at both ends of the emitter fingers electrically connected by the same emitter wirings occupy in a plane orthogonal to the thickness-wise direction of the semiconductor substrate and the wiring board, are included in areas, which the through holes in the wiring board occupy."

Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The undescribed subject matter of the claimed invention is the language, "wherein areas, which emitter fingers except emitter fingers at both ends of the emitter fingers electrically connected by the same emitter wirings occupy in a plane orthogonal to the thickness-wise direction of the semiconductor substrate and the wiring board, are included in areas, which the through holes in the wiring board occupy."

To determine adequacy of written description for original claims MPEP 2163IIA2(a) (redacted) instructs:

> (i) For Each Claim Drawn to a Single Embodiment Or Species:
> (A) Determine whether the application describes an actual reduction to practice of the claimed invention.
> (B) If the application does not describe an actual reduction to practice, determine whether the invention is complete as evidenced by a reduction to drawings or structural chemical formulas that are sufficiently detailed to show that applicant was in possession of the claimed invention as a whole.
> (C) If the application does not describe an actual reduction to practice or reduction to drawings or structural chemical formula as discussed above, determine whether the invention has been set forth in terms of distinguishing identifying characteristics as evidenced by other descriptions of the invention that are sufficiently detailed to show that applicant was in possession of the claimed invention.
> (1) Determine whether the application as filed describes the complete structure (or acts of a process) of the claimed invention as a whole.
> (2) If the application as filed does not disclose the complete structure (or acts of a process) of the claimed invention as a whole, determine whether the specification discloses other relevant identifying characteristics sufficient to describe the claimed invention in such full, clear, concise, and exact terms that a skilled artisan would recognize applicant was in possession of the claimed invention. Any claim to a species that does not meet the test described under at least one of (a), (b), or (c) must be rejected as lacking adequate written description under 35 U.S.C. 112, para. 1.

ii) For each claim drawn to a genus:
The written description requirement for a claimed genus may be satisfied through sufficient description of a representative number of species by actual reduction to practice (see i)(A), above), reduction to drawings (see i)(B), above), or by disclosure of relevant, identifying characteristics, i.e., structure or other physical and/or chemical properties, by functional characteristics coupled with a known or disclosed correlation between function and structure, or by a combination of such identifying characteristics, sufficient to show the applicant was in possession of the claimed genus (see i)(C), above).

Regarding claims 11, the instant application does not describe an actual reduction to practice of the claimed invention; the invention is not complete as evidenced by a reduction to drawings or structural chemical formulas that are sufficiently detailed to show that applicant was in possession of the claimed invention as a whole; the invention has not been set forth in terms of distinguishing identifying characteristics as evidenced by other descriptions of the invention that are sufficiently detailed to show that applicant was in possession of the claimed invention; the application as filed does not describe the complete structure of the claimed invention as a whole; and the specification does not disclose other relevant identifying characteristics sufficient to describe the claimed invention in such full, clear, concise, and exact terms that a skilled artisan would recognize applicant was in possession of the claimed invention.

The instant application does not describe sufficient description of a representative number of species by actual reduction to practice, reduction to drawings, or by disclosure

of relevant, identifying characteristics, i.e., structure or other physical and/or chemical properties, by functional characteristics coupled with a known or disclosed correlation between function and structure, or by a combination of such identifying characteristics, sufficient to show the applicant was in possession of the claimed genus.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4, 5/3, 6/3 and 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4 the language, "and heat flow one-dimensionally ..." appears to be grammatically incorrect and is confusing.

In claims 8 and 9 the scope of the term "calorific values" is unclear because the term does not appear to be given its usual meaning as defined in the U.S. Manual of Classification, Class 374/36 - "the amount of heat produced by burning a given amount of a tested combustible material." Further, the term does not appear to be otherwise clearly defined in the disclosure, and one of ordinary skill in the art, in view of the

prior art and the status of the art, would not otherwise be reasonably apprised of the scope of the term.

There is insufficient antecedent basis for the following:

Claim 3, "the thickness-wise direction" ... "of the semiconductor substrate";

Claims 8 and 9, "the thickness-wise direction" (all occurrences), "the distribution density of calorific values," and, "the distribution density";

Claim 10, "the through holes extending through the wiring board," "the through holes" ... "of the wiring board," "the through holes of the multilayer wiring board";

Claim 11, "both ends of the emitter fingers electrically connected by the same emitter wirings," "the same emitter wirings," "the thickness-wise direction of the semiconductor substrate," "both ends";

Claim 13, "the multilayer wiring board," "the thickness-wise direction."

In claim 11 there is ambiguous antecedent basis for the term "therein."

In claim 12 the scope of the term "finger-like" cannot be determined because the common qualities that distinguish the individual members of the class *like* as an identifiable class

are not recited in the claims, and they cannot otherwise be determined.

In claim 12, the scope of the term "offset" is unclear because the term appears to be given a meaning repugnant to its usual meaning.

Claim 11 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06.

In the rejections infra, reference labels are generally recited only for the first recitation of identical elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-10 are rejected under 35 U.S.C. 102(a) as being anticipated by Shirakawa (1077494).

At column 10, line 15 to column 11, line 35, column 18, line 9 to column 20, line 6, and column 22, lines 52 to column 23, line 7, Shirakawa teaches a multilayer (layers 13 and 12) wiring board 13 having through holes 10b in a thickness-wise direction, wherein a semiconductor substrate 1 mounted on the multilayer wiring board has through holes 10a in a thickness-wise direction thereof, and entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas, which the through holes in the multilayer wiring board occupy, wherein conductive layers 11 are formed on side surfaces of the through holes, a semiconductor element 1 is mounted in which conductive layers 11 are formed on side surfaces of the through holes, and wirings 11, which connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface 12 of the multilayer wiring board,

on which the semiconductor substrate is not mounted, in this order, a multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly (in some measure or degree) overlap areas which the through holes in the multilayer wiring board occupy, a multilayer wiring board having a through hole or holes in a thickness-wise direction, wherein respective heating areas 11 inside a semiconductor substrate mounted on the multilayer wiring board are included in areas, which the single or plural through holes in the multilayer wiring board occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate, a multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and heat flow one- dimensionally through the through holes in the semiconductor substrate and the through holes in the multilayer wiring board in the thickness-wise direction when heat flows out

to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board, a multilayer wiring board having through holes in a thickness-wise direction, wherein the distribution density of calorific values in a plane orthogonal to the thickness-wise direction of a semiconductor substrate mounted on the multilayer wiring board inherently substantially coincides with the distribution density in a plane orthogonal to the thickness-wise direction of the through holes, a multilayer wiring board having through holes in a thickness-wise direction, wherein the distribution density of calorific values in a plane orthogonal to the thickness-wise direction of a semiconductor substrate mounted on the multilayer wiring board inherently substantially coincides with the distribution density of large and small cross-sectional areas in a plane orthogonal to the thickness-wise direction of the through holes, a wiring board, wherein a semiconductor substrate having through holes, which are connected to emitter wirings 4 connected to emitters of heterojunction bipolar transistors and extend through the semiconductor substrate in a thickness-wise direction and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and

the through holes in the semiconductor substrate and the through holes extending through the wiring board in a thickness-wise direction are connected to each other, and wherein conductive layers are provided on sides of or inside of the through holes in the semiconductor substrate and the wiring board, and areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas, which the through holes in the multilayer wiring board occupy.

Claim 12 is rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art.

In the specification, at pages 12-22, applicant teaches as conventional a semiconductor device 1 including a plurality of finger-like emitter electrodes 7, and at least one via hole 5 arranged in rows in a first direction on a semiconductor substrate, in which semiconductor device the emitter electrodes are connected to a conductive layer 6 formed on a back surface opposite to that surface, on which the electrodes are formed, through the via hole, and in which semiconductor device rows (not labeled but illustrated in Figure 11) comprising the emitter electrodes or source electrodes, and the via hole are arranged in parallel in a second direction orthogonal to the

first direction, and the via holes are positionally offset (in the second direction) from one another among adjacent rows, and adjacent rows are positionally offset (in the second direction) from one another.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art as applied to claim 12, and further in combination with Shirakawa (1077494).

Applicant does not appear to explicitly teach as conventional wherein the multilayer wiring board has through holes formed on sides thereof or inside thereof with a conductive layer, and areas, which the via hole of the semiconductor device occupies, overlap areas, which the through holes of the multilayer wiring board occupy in a plane orthogonal to the thickness-wise direction.

Nonetheless, as cited supra, Shirakawa teaches wherein a multilayer wiring board 13 has through holes 10b formed on sides thereof or inside thereof with a conductive layer 11, and areas, which the via hole of the semiconductor device 1 occupies, overlap areas, which the through holes of the multilayer wiring board occupy in a plane orthogonal to the thickness-wise direction.

Moreover, it would have been obvious to combine the product of Shirakawa with the product of applicant's admitted prior art because it would facilitate heat dissipation.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
2-Sep-03